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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,258	08/24/2001	James M. Derderian	4831US (01-0105)	2185

24247 7590 11/19/2007

TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	**PAPER NUMBER**
2822	

NOTIFICATION DATE	DELIVERY MODE
11/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

Office Action Summary	Application No.	Applicant(s)	
	09/939,258	DERDERIAN, JAMES M.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-25,28-35,53 and 54* is/are pending in the application.

4a) Of the above claim(s) *9,24 and 29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-8,10-23,25,28,30-35,53 and 54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3 pages*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5-8, 10-23, 25, 28, 31, 32, 34, 35, 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hikita (6724084) and Eldridge (6835898).

At column 11, lines 24-44; column 12, lines 28-33; column 12, line 53 to column 13, line 52; column 14, lines 3-18; column 14, line 60 to column 15, line 6; column 15, lines 27-39; column 18, line 34 to column 19, line 38; and column 20, lines 33-36, Hikita discloses the following:

Re claim 1: A semiconductor device assembly, comprising: at least one semiconductor device 1; and at least one inherently compressible spacer BD protruding from an active surface of the at least one semiconductor device, the at least one compressible spacer inherently defining a distance the active surface of the at least one semiconductor device is to be spaced apart from a back side of another semiconductor device 2 to be positioned in superimposed relation with the at least one semiconductor device.

Re claim 5: The semiconductor device assembly re claim 1, comprising a plurality of spacers that are arranged to stably support the another semiconductor device.

Re claim 6: The semiconductor device assembly re claim 1, further comprising: the another semiconductor device positioned adjacent the at least one compressible spacer, opposite from the at least one semiconductor device.

Re claim 7: The semiconductor device assembly re claim 6, further comprising: adhesive material 3 between the at least one semiconductor device and the another semiconductor device.

Re claim 8: The semiconductor device assembly re claim 7, wherein the adhesive material is located between adjacent spacers.

Re claim 10: The semiconductor device assembly re claim 1, wherein the at least one compressible spacer comprises electrically conductive material.

Re claim 11: The semiconductor device assembly re claim 10, wherein the at least one compressible spacer communicates with a "ground" plane of the at least one semiconductor device.

Re claim 12: The semiconductor device assembly re claim 1, further comprising: a substrate 14 with which at least one semiconductor device is associated.

Re claim 13: The semiconductor device assembly re claim 12, wherein the substrate comprises at least one of a circuit board, an interposer, a semiconductor device, and leads.

Re claim 14: The semiconductor device assembly re claim 12, wherein at least one bond pad 12 of the at least one semiconductor device is in communication with a corresponding contact area of the substrate.

Re claim 15: The semiconductor device assembly re claim 14, further comprising: at least one discrete conductive element 13 extending from the at least one bond pad, over an active surface of the at least one semiconductor device, to the corresponding contact area.

Re claim 16: The semiconductor device assembly re claim 15, wherein heights of the at least one compressible spacer exceeds a maximum height the at least one discrete conductive element protrudes above the active surface.

Re claim 17: The semiconductor device assembly re claim 1, wherein the at least one compressible spacer is secured to noncircuit bond pads 52 of the at least one semiconductor device.

Re claim 18: A semiconductor device assembly, comprising: a substrate; a first semiconductor device associated with the substrate, bond pads of the first semiconductor device in communication with corresponding contact areas of the substrate; mutually laterally spaced discrete spacers

positioned on and protruding from an active surface of the first semiconductor device, at least one spacer of the mutually laterally discrete spacers being in communication with a "ground" or reference voltage plane of the first semiconductor device; and a second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers, the at least one spacer establishing communication between the back side of the second semiconductor device and the ground or reference voltage plane.

Re claim 19: The semiconductor device assembly re claim 18, wherein the substrate comprises one of a circuit board, an interposer, another semiconductor device, and leads.

Re claim 20: The semiconductor device assembly re claim 18, wherein the bond pads and the corresponding contact areas communicate by way of discrete conductive elements positioned therebetween.

Re claim 21: The semiconductor device assembly re claim 20, wherein the discrete conductive elements comprise at least one of bond wires, tape-automated bond elements, and thermocompression bonded leads.

Re claim 22: The semiconductor device re claim 18, wherein the mutually laterally spaced discrete spacers are secured to noncircuit bond pads of the first semiconductor device.

Re claim 23: The semiconductor device assembly re claim 22, wherein the mutually laterally spaced discrete spacers comprise conductive material.

Re claim 25: The semiconductor device assembly re claim 23, wherein the mutually laterally spaced discrete spacers are in communication with a ground or reference voltage plane of the first semiconductor device.

Re claim 28: The semiconductor device assembly re claim 18, wherein at least one of the mutually laterally spaced discrete spacers is compressible.

Re claim 30: The semiconductor device assembly re claim 18, wherein the bond pads communicate with the corresponding contact areas of the substrate by way of discrete conductive elements positioned therebetween.

Re claim 31: The semiconductor device assembly re claim 18, further comprising: an adhesive layer between the first semiconductor device and the second semiconductor device.

Re claim 32: The semiconductor device assembly re claim 31, wherein at least some of the mutually laterally spaced discrete spacers extend through the adhesive layer.

Re claim 34: The semiconductor device assembly re claim 18, further comprising: an encapsulant material 3 substantially covering the first semiconductor device, the second semiconductor device, discrete conductive

elements, and portions of the substrate located adjacent to the first semiconductor device.

Re claim 35: The semiconductor device assembly re claim 18, further comprising: at least one external connective element 14 carried by the substrate and in electrical communication with at least one corresponding contact area of the substrate.

Re claim 53: The semiconductor device assembly re claim 1, wherein the at least one compressible spacer is secured to a contact pad of the at least one semiconductor device.

Re claim 54: The semiconductor device assembly re claim 18, wherein the at least one spacer is secured to a contact pad of at least one of the first semiconductor device and the second semiconductor device.

To further clarify, Hikita discloses an inherently compressible spacer because the term "compressible" merely limits the scope of the claims to the intended use of the spacer and does not appear to result in a structural difference between the claimed spacer and the spacer of the applied prior art. Further, because the spacer of Hikita appears to have the same structure as the claimed spacer, it appears to be capable of being used for the intended use, and the intended use does not patentably distinguish the claimed spacer from the spacer of Hikita. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte

Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

To further clarify the disclosure of the second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers, the at least one spacer establishing communication between the back side of the second semiconductor device and the ground or reference voltage plane, it is noted that the term "back" is a relative term defined as "the reverse side," (The American Heritage® Dictionary of the English Language: Fourth Edition. 2000) and the side of the second semiconductor

device of Hikita facing the active surface is inherently the reverse side of the second semiconductor device relative to the side of the second semiconductor device opposite the side facing the active surface of the first semiconductor device. To continue to afford applicant the benefit of compact prosecution, it is noted that the term "back side" is not defined in the instant specification, nor is the scope of the term otherwise limited to a non-active side of a semiconductor device. In any case, the following limitations are statements of intended use:

Re claim 1: to be spaced apart from a back side of another semiconductor device to be positioned in superimposed relation with the at least one semiconductor device.

Re claim 5: to stably support the another semiconductor device.

Therefore, the scope of claims 1 and 5 is not structurally limited to another semiconductor device and the statements of intended use do not appear to otherwise result in a structural difference between the claimed device and the device of Hikita. Further, because the device of Hikita appears to have the same structure as the claimed device, it appears to be capable of being used for the intended uses, and the statements of intended use do not patentably distinguish the claimed device from the device of Hikita. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548

(BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

However, Hikita does not appear to explicitly disclose resiliently compressible spacers.

Nonetheless, at column 58, lines 31-43; column 59, lines 24-28 and 38-51; column 59, line 62 to column 60, line 8; column 61, lines 23-34; column 62, lines 26-41; column 77, lines 8-45; column 97, line 66 to column 98, line 18; column 132, line 66 to column 133, line 12; and column 133, line 41 to column 134, line 176, Eldridge discloses resiliently compressible spacers "contact structures." In addition, it would have been obvious to

combine this disclosure of Eldridge with the disclosure of Hikita by substituting or combining the spacers of Eldridge for or with the spacers of Hikita because, as disclosed by Eldridge as cited, since the spacers have high aspect (height: width) ratios, cleaning (e.g., of solder flux) and inspectability would be increased as compared with traditional solder-bump type flip-chip surface mount processes such as the spacers of Hikita; the same spacers can be used for demountable or permanent attachment of the electronic component; the spacers can be used as a standard means of interconnect between substrates and components which have matching patterns of terminals; the self-planarizing feature of the spacers (i.e., resilient spacers originating from different levels can all be made to terminate in a common plane) affords many opportunities not present with prior art interconnection techniques; the spacers can be bonded to a terminal that is skewed with respect to other terminals; the spacers have high electrical conductivity (low resistivity) in order that constriction resistance and bulk resistance are low; the spacers have high thermal conductivity so that joule heat (I^2 R) is rapidly conducted away from the spacers interface; the spacers have softness, so that a-spots are large, thereby providing low constriction resistance; the spacers have high hardness for low mechanical wear; the spacers have high strength to provide the ability to serve as a spacer and cantilever beam to give low mechanical wear; the spacers have high

noble metal content for extended shelf life, low electrical noise and excellent reliability; the spacers have the ability to form extremely thin lubricating films, but not an excess of frictional polymer; and the spacers have low cost.

Also, Hikita and Eldridge do not appear to explicitly disclose wherein heights of the at least one resiliently compressible spacer exceeds a maximum height the at least one discrete conductive element protrudes above the active surface.

Notwithstanding, as reasoned from well established legal precedent, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that, **in view of the applied prior art**, the dimensions are for a particular **unobvious** purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular **unobvious** purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777

(Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 16, 30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita and Eldridge as applied to claims 15 and 18, and further in combination with Pu (6593662).

Hikita and Eldridge do not appear to explicitly disclose the following:

Re claim 16: The semiconductor device assembly re claim 15, wherein heights of the at least one compressible spacer exceeds a maximum height the at least one discrete conductive element protrudes above the active surface.

Still, at column 1, lines 25-48; column 2, lines 17-20 and 30-42; and column 3, line 66 to column 5, line 32, Pu discloses wherein heights of at least one spacer 204b, 220, 204c exceeds a maximum height an at least one discrete conductive element 210a protrudes above a surface 201. Moreover, it would have been obvious to combine this disclosure of Pu with the disclosure of Hikita and Eldridge because, as disclosed by Pu, it would facilitate provision of a stacked-die package structure capable of stacking dies having substantially the same size and bonding pads around the peripheral sides of the dies.

Also, Hikita and Eldridge do not appear to explicitly disclose the following:

Re claim 30: The semiconductor device assembly re claim 18, wherein bond pads of the second semiconductor device communicate with the corresponding contact areas of the substrate by way of discrete conductive elements positioned therebetween.

Re claim 33: The semiconductor device assembly re claim 18, further comprising: at least one additional semiconductor device positioned over the second semiconductor device.

Regardless, as cited, Pu discloses wherein bond pads 222 of a second semiconductor device 208 communicate with corresponding contact areas of a substrate 202 by way of discrete conductive elements 210b positioned therebetween and at least one additional semiconductor device "a number of dies" positioned over the second semiconductor device. Furthermore, it would have been obvious to combine this disclosure of Pu with the disclosure of Hikita and Eldridge because it would facilitate provision of a stacked-die package structure capable of stacking a number of dies having substantially the same size and bonding pads around the peripheral sides of the dies.

Applicant's amendment and remarks filed 8-27-7 have been fully considered, are addressed by the rejections supra, and are further addressed infra.

Applicant submits, "FIGs. 10A-10D of the as-filed specification depict how the resiliently compressible spacers (40a-40d) may be used to facilitate

semiconductor device assembly. *Id*,, paragraph [0047]," and, "FIGs. 10A-10D of the as-filed specification specifically show non-limiting examples of how resiliently compressible spacers (40a-40d) may be used in a semiconductor device assembly. *Id.*, paragraph [0047]."

These submissions are respectfully deemed traversed because paragraph [0047] does not appear to depict how the resiliently compressible spacers (40a-40d) may be used to facilitate semiconductor device assembly or show non-limiting examples of how resiliently compressible spacers (40a-40d) may be used in a semiconductor device assembly.

Also, applicant contends, "neither Hikita nor Eldridge teaches or suggests a spacer that defines a distance that the active surface of at least one semiconductor device is to be spaced apart from the back side of another semiconductor device to be positioned in superimposed relation with the at least one semiconductor device. Rather, both Hikita and Eldridge teach structures positioned between opposing active surfaces of semiconductor dice."

This contention is respectfully traversed because an alleged disclosure of Hikita of structures positioned between opposing active surfaces of semiconductor dice would not necessarily preclude the disclosure of Hikita of a spacer that defines a distance that the active surface of at least one semiconductor device is to be spaced apart from the back side of another

semiconductor device to be positioned in superimposed relation with the at least one semiconductor device.

Applicant further asserts, "Because Hikita is limited to a stacked device with active surfaces of a primary chip 1 and secondary chip 2 facing each other, Hikita does not teach semiconductor devices positioned in superimposed relation," and, "Because the description of Eldridge is limited to contact structures used to connect electronic components with active surface facing one another, Eldridge does not teach or suggest electronic components positioned in superimposed relation to one another."

These assertions are respectfully traversed because they are non-sequiturs. Specifically, alleged disclosures of Hikita limited to a stacked device with active surfaces of a primary chip 1 and secondary chip 2 facing each other and to contact structures used to connect electronic components with active surface facing one another would not necessarily preclude the disclosures of Hikita of semiconductor devices positioned in superimposed relation or electronic components positioned in superimposed relation to one another.

In addition, applicant alleges, "one of skill in the art would not be motivated to combine the teachings of Hikita relating to dummy bumps BD1 and BD2 that protect the chips from stress caused by resin sealing with the teachings of Eldridge relating to electrical contacts," and, "one of skill in the

art would not be motivated to combine the teachings of Hikita relating to non-conductive dummy bumps configured to support stacked IC chips with the teachings of Eldridge relating to contact structures that facilitate electrical connection between electronic devices."

These allegations are respectfully traversed because Hikita is not necessarily applied for a disclosure that one of skill in the art would be motivated to combine the teachings of Hikita relating to dummy bumps BD1 and BD2 that protect the chips from stress caused by resin sealing with the teachings of Eldridge relating to electrical contacts. Furthermore, it is respectfully submitted that motivation to combine the applied prior art is unnecessary - "The obviousness inquiry cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents." KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007). Similarly, as expounded in Ex parte Jones, 62 USPQ2d 1206 (BdPatApp&Int 2001), "The applicant and the examiner have apparently assumed that there always must be 'motivation' to combine teachings of the prior art to support a rejection based on §103(a). The assumption is not correct. The word 'motivation' or a word similar to 'motivation' does not appear in 35 U.S.C. § 103(a). While a finding of 'motivation' supported by substantial evidence probably will support

combining teachings of different prior art references to establish a *prima facie* obviousness case, it is not always necessary. For example, where a claimed apparatus requiring Phillips head screws differs from a prior art apparatus describing the use of flathead screws, it might be hard to find motivation to substitute flathead screws with Phillips head screws to arrive at the claimed invention. However, the prior art would make it more than clear that Phillips head screws and flathead screws are viable alternatives serving the same purpose. Hence, the prior art would 'suggest' substitution of flathead screws for Phillips head screws albeit the prior art might not 'motivate' use of Phillips head screws in place of flathead screws. What must be established to sustain an obviousness rejection is a legally sufficient rationale as to why the claimed subject matter, as a whole, would have been obvious notwithstanding a difference between claimed subject matter and a reference which is prior art under 35 U.S.C. § 102. Once a difference is found to exist, then the examiner must articulate a legally sufficient rationale in support of a §103(a) rejection." To this end, in the instant Office action, legally sufficient rationale as to why the claimed subject matter, as a whole, would have been obvious has been provided.

Applicant also argues, "Neither Hikita nor Eldridge teaches or suggests a second semiconductor device comprising a back side positioned on mutually laterally spaced discrete spacers. Rather, both Hikita and Eldridge

teach semiconductor devices configured with active surfaces facing each other as described with respect to claim 1."

This argument is respectfully traversed because it is a non-sequitur. First, the statement, "both Hikita and Eldridge teach semiconductor devices configured with active surfaces facing each other as described with respect to claim 1," is an admission that the applied prior art discloses the claimed invention. Second, the alleged disclosures of Hikita and Eldridge of semiconductor devices configured with active surfaces facing each other would not necessarily preclude the disclosures of Hikita of a second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers as evidenced by the following: Inagaki (JP59108341), English abstract, "back sides as active regions"; Zommer (6162665), column 4, line 63, column 5, lines 23-24, column 5, line 67 to column 6, line 1, column 6, lines 10-11 and column 7, lines 9-10, "active devices on the backside"; Adamic (6124179), column 4, line 26 and column 15, line 61, "backside ohmic contacts or active junctions"; and Temple (5654226), column 2, lines 64-65, "the device wafer 10 may be partially processed on the backside to create a plurality of active areas 14."

Relatedly, applicant proposes, "relative to the 'active surface' of the semiconductor device, the 'back side' of the semiconductor device refers an [sic] opposite surface."

This proposition is respectfully deemed unpersuasive because it is ambiguously unclear. Specifically, it is unclear which semiconductor device(s) is referred to by the language, "the semiconductor device." In any case, the scope of the instant claims is not limited to wherein, relative to the active surface of the semiconductor device, the back side of the semiconductor device refers to an opposite surface.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR:

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
2-Nov-07